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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,393	09/19/2006	Kazumasa Tanida	AI-425NP	8907

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,393	TANIDA ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 9/19/06.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/593393 Attorney's Docket #: AI-425NP
Filing Date: 9/19/2006; claimed foreign priority to 9/29/2004

Applicant: Tanida et al.

Examiner: Alexander Williams

This application is a 371 of PCT/JP05/14294 filed 8/04/2005.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences btween the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Saito Koichi (Japan Patent Publication # 09-082759).

1. Koichi (figures 1A to 2B) specifically figure 2B show a wiring board **21,22** to which a semiconductor chip **32**is to be bonded while directing a surface of the semiconductor chip toward the wiring board, the wiring board comprising: a connection electrode **27** formed on a bonding surface to which the semiconductor chip is to be bonded, the connection electrode being for a connection with the semiconductor chip; an insulating film **41** formed on the bonding surface, the insulating film having an opening to expose the connection electrode; and a low-melting-point metallic part **28** provided on the connection electrode in the opening, the low-melting-point metallic part being made of a low-melting-point metallic material whose solidus temperature is lower than that of the connection electrode.

2. A wiring board according to claim 1, Koichi show wherein a volume of an inside of the opening is greater than a sum of a volume of a connection electrode and a volume of the low-melting-point metallic part.

3. Koichi (figures 1A to 2B) specifically figure 2B show a semiconductor device comprising: a wiring board **21,22**; and a semiconductor chip **32** having a projection electrode **33** formed on a surface on which a functional element is formed, the projection electrode being electrically connected to the functional element, the semiconductor chip being bonded to a bonding surface of the wiring board with the surface of the semiconductor chip facing the bonding surface; the wiring board including: a connection electrode **27** formed on the bonding surface, the connection electrode being used to make a connection with the semiconductor chip; an insulating film formed on the bonding surface, the insulating film **41** having an opening to expose the connection electrode; and a low-melting-point metallic part provided on the connection electrode in the opening, the low-melting-point metallic part being made of a low-melting-point metallic material whose solidus temperature is lower than that of the connection electrode.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by (Japan Patent Publication # 49-33564).

1. (JP 49-33564) show a wiring board **5** to which a semiconductor chip is to be bonded while directing a surface of the semiconductor chip toward the wiring board, the wiring board comprising: a connection electrode **6** formed on a bonding surface to which the semiconductor chip is to be bonded, the connection

electrode being for a connection with the semiconductor chip; an insulating film **7** formed on the bonding surface, the insulating film having an opening to expose the connection electrode; and a low-melting-point metallic part **9** provided on the connection electrode in the opening, the low-melting-point metallic part being made of a low-melting-point metallic material whose solidus temperature is lower than that of the connection electrode.

2. A wiring board according to claim 1, (JP 49-33564) show wherein a volume of an inside of the opening is greater than a sum of a volume of a connection electrode and a volume of the low-melting-point metallic part.

3. (JP 49-33564) show a semiconductor device comprising: a wiring board **5**; and a semiconductor chip **(inherent)** having a projection electrode **1** formed on a surface on which a functional element **8** is formed, the projection electrode being electrically connected to the functional element, the semiconductor chip being bonded to a bonding surface of the wiring board with the surface of the semiconductor chip facing the bonding surface; the wiring board including: a connection electrode **6** formed on the bonding surface, the connection electrode being used to make a connection with the semiconductor chip; an insulating film **7** formed on the bonding surface, the insulating film having an opening to expose the connection electrode; and a low-melting-point metallic part provided on the connection electrode in the opening, the low-melting-point metallic part being made of a low-melting-point metallic material whose solidus temperature is lower than that of the connection electrode.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Matsuki et al. (U.S. Patent Application Publication # 2003/0151141 A1).

1. Matsuki et al. (figures 1 to 53B) specifically figures 31A and 31B show a wiring board **1** to which a semiconductor chip is

to be bonded while directing a surface of the semiconductor chip toward the wiring board, the wiring board comprising: a connection electrode **3** formed on a bonding surface to which the semiconductor chip is to be bonded, the connection electrode being for a connection with the semiconductor chip; an insulating film **2** formed on the bonding surface, the insulating film having an opening to expose the connection electrode; and a low-melting-point metallic part **5,5a,5b,8a** provided on the connection electrode in the opening, the low-melting-point metallic part being made of a low-melting-point metallic material whose solidus temperature is lower than that of the connection electrode.

2. A wiring board according to claim 1, Matsuki et al. show wherein a volume of an inside of the opening is greater than a sum of a volume of a connection electrode and a volume of the low-melting-point metallic part.

3. Matsuki et al. (figures 1 to 53B) specifically figures 31A and 31B show a semiconductor device comprising: a wiring board **1**; and a semiconductor chip **(36,36 and structure)** having a projection electrode **35a(35)** formed on a surface on which a functional element **42** is formed, the projection electrode being electrically connected to the functional element, the semiconductor chip being bonded to a bonding surface of the wiring board with the surface of the semiconductor chip facing the bonding surface; the wiring board including: a connection electrode **3** formed on the bonding surface, the connection electrode being used to make a connection with the semiconductor chip; an insulating film **2** formed on the bonding surface, the

insulating film having an opening to expose the connection electrode; and a low-melting-point metallic part **5,5a,5b,8a** provided on the connection electrode in the opening, the low-melting-point metallic part being made of a low-melting-point metallic material whose solidus temperature is lower than that of the connection electrode.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/778,778,734,737,738,692,693,780,782,746,e23.068,e23.021,e21.512	1/30/08
Other Documentation: foreign patents and literature in 257/778,778,734,737,738,692,693,780,782,746,e23.068,e23.021,e21.512	1/30/08
Electronic data base(s): U.S. Patents EAST	1/30/08

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
1/30/08